FIG. 1A

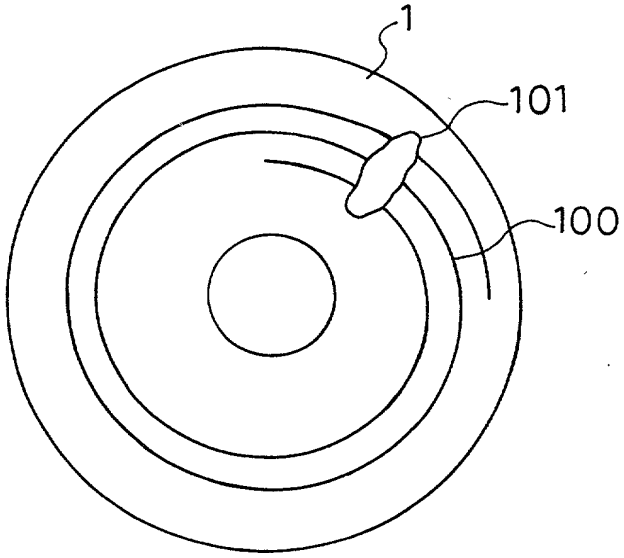


FIG. 1B

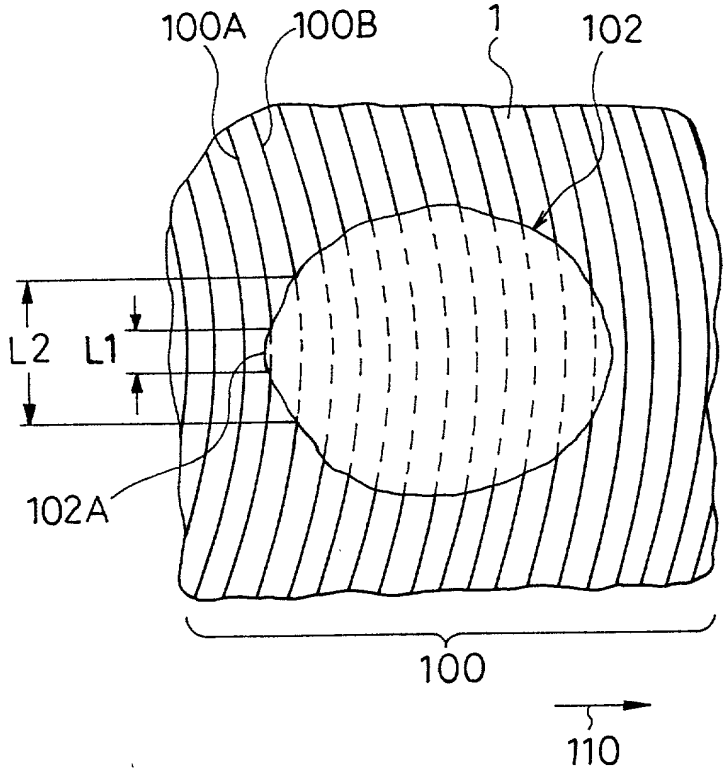


FIG. 2A

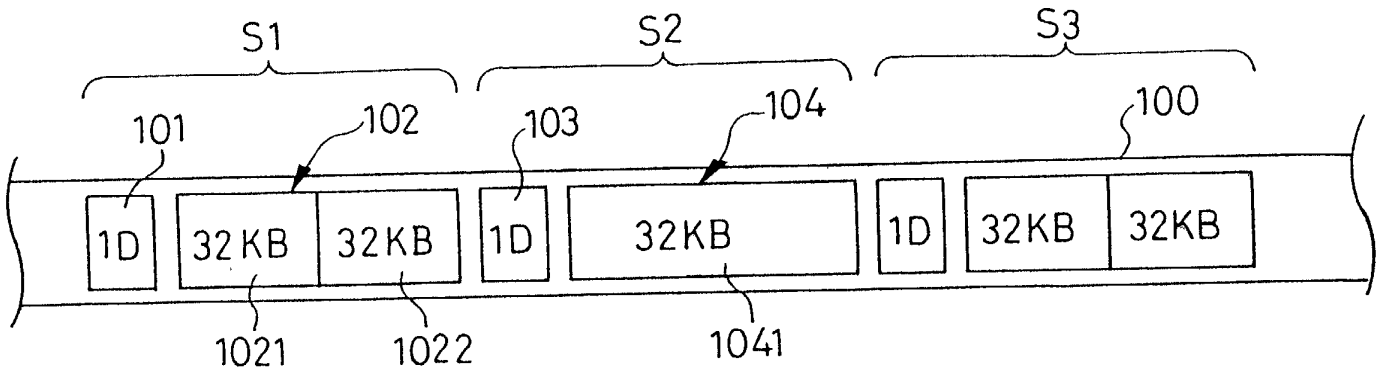


FIG. 2B

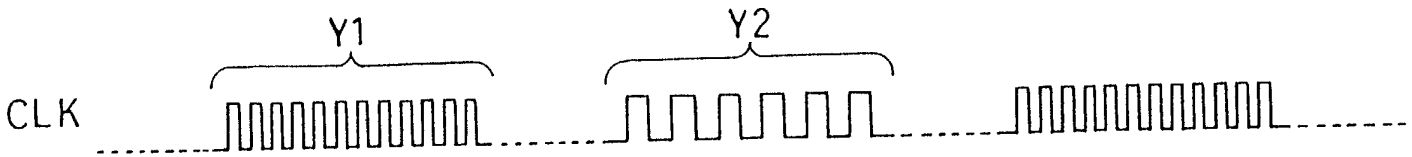


FIG. 2C

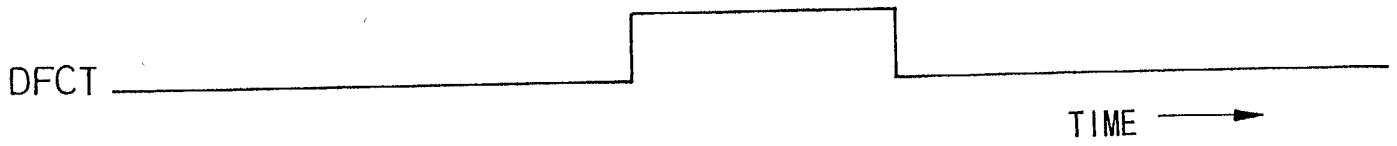


FIG. 3

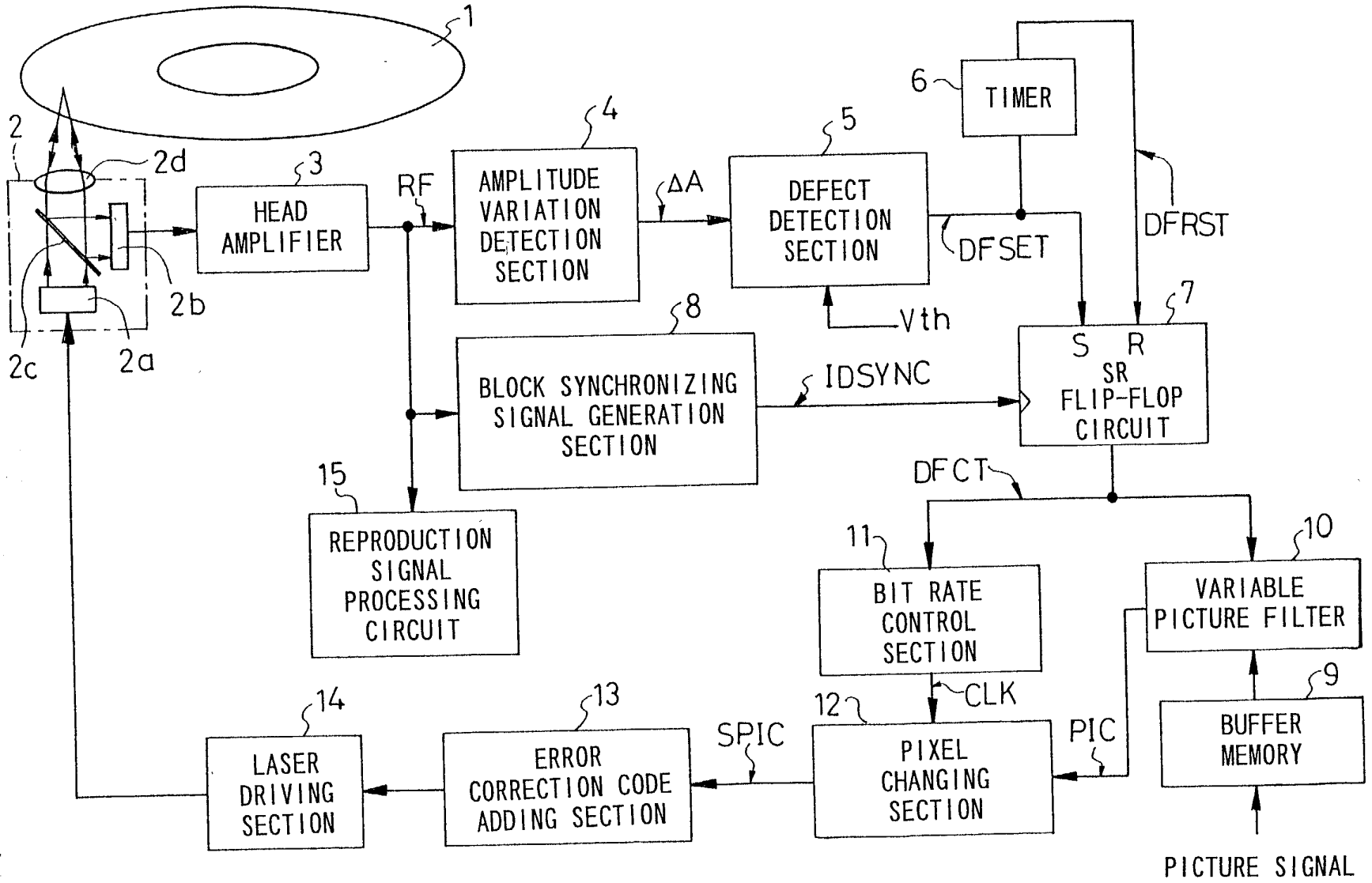

1
2
2d
2b
2c
2a
3
HEAD AMPLIFIER
RF
4
AMPLITUDE VARIATION DETECTION SECTION
ΔA
5
DEFECT DETECTION SECTION
Vth
DFSET
6
TIMER
DFRST
7
S R
SR FLIP-FLOP CIRCUIT
8
BLOCK SYNCHRONIZING SIGNAL GENERATION SECTION
IDSYNC
15
REPRODUCTION SIGNAL PROCESSING CIRCUIT
DFCT
11
BIT RATE CONTROL SECTION
CLK
10
VARIABLE PICTURE FILTER
9
BUFFER MEMORY
PICTURE SIGNAL
12
PIXEL CHANGING SECTION
PIC
SPIC
13
ERROR CORRECTION CODE ADDING SECTION
14
LASER DRIVING SECTION

FIG. 4A

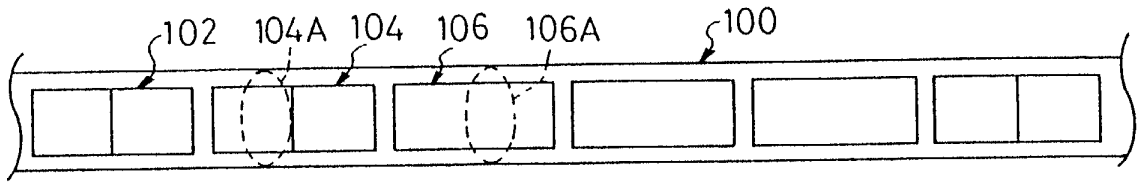


FIG. 4B BLOCK SYNCHRONIZING SIGNAL IDSYNC

FIG. 4C OUTPUT SIGNAL RF

FIG. 4D DECREMENT SIGNAL ΔA OF OUTPUT SIGNAL RF

FIG. 4E SET PULSE DFSET

FIG. 4F RESET PULSE DFRST

FIG. 4G DEFECT DETERMINATION SIGNAL DFCT

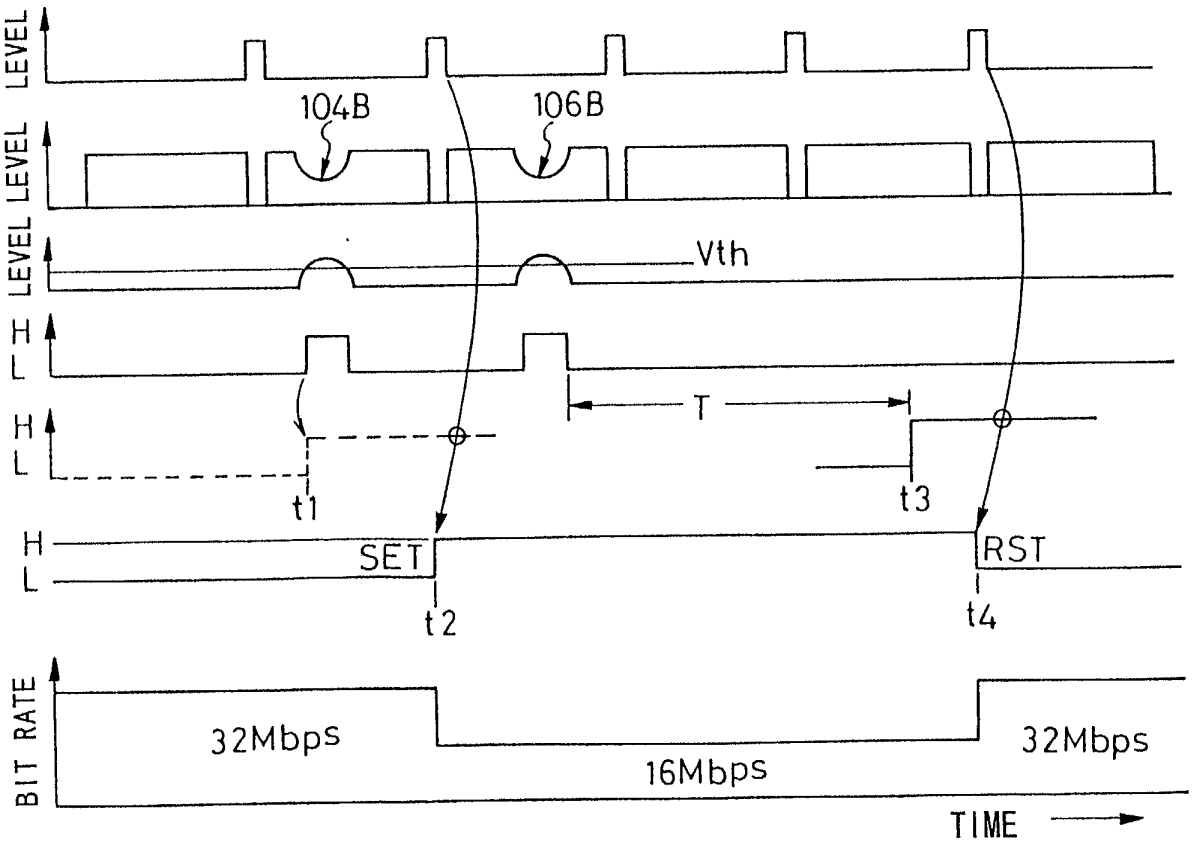


FIG. 4H BIT RATE

FIG. 5A

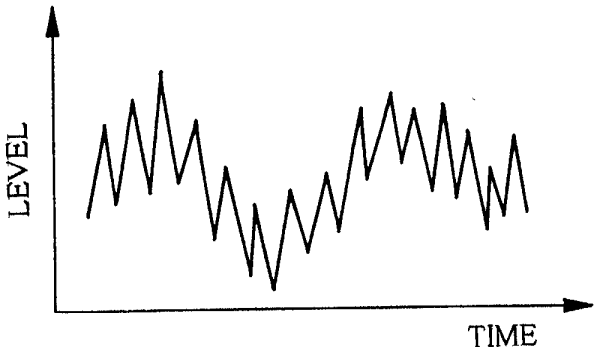


FIG. 5B

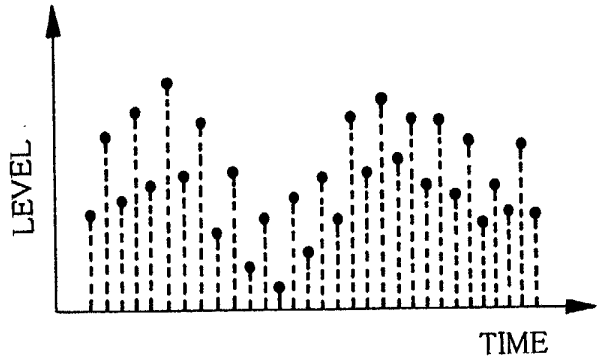


FIG. 5C

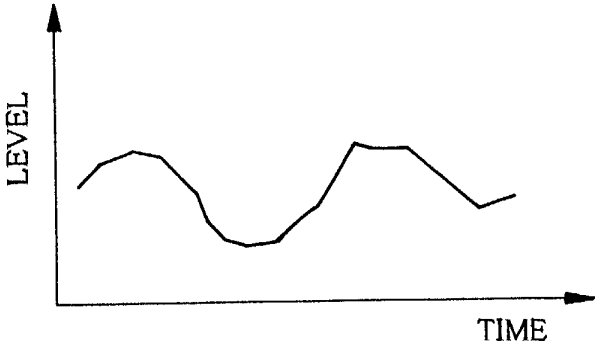


FIG. 5D

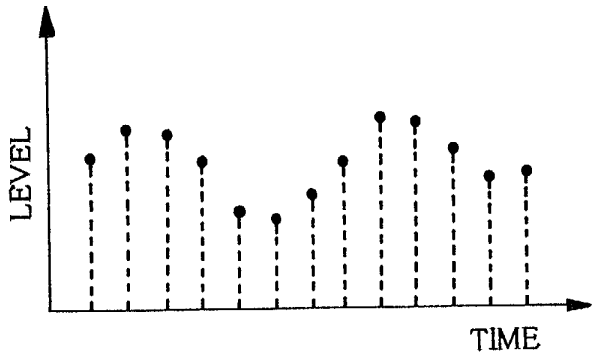
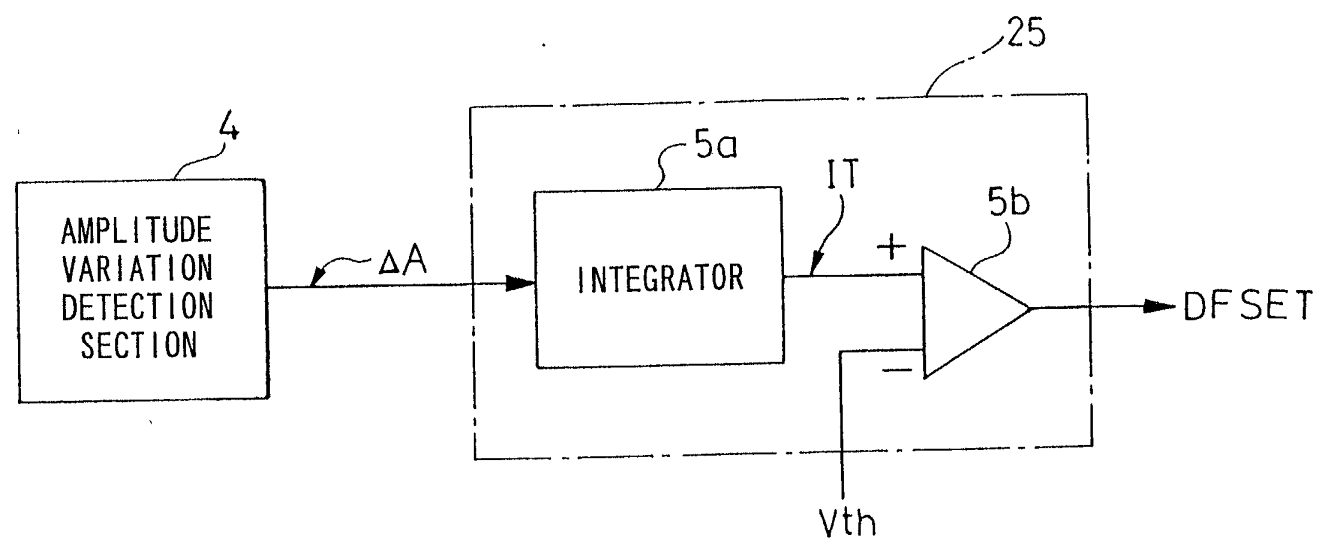


FIG. 6



4
AMPLITUDE VARIATION DETECTION SECTION
ΔA
25
5a
INTEGRATOR
IT
+
−
5b
DFSET
Vth

FIG. 7A

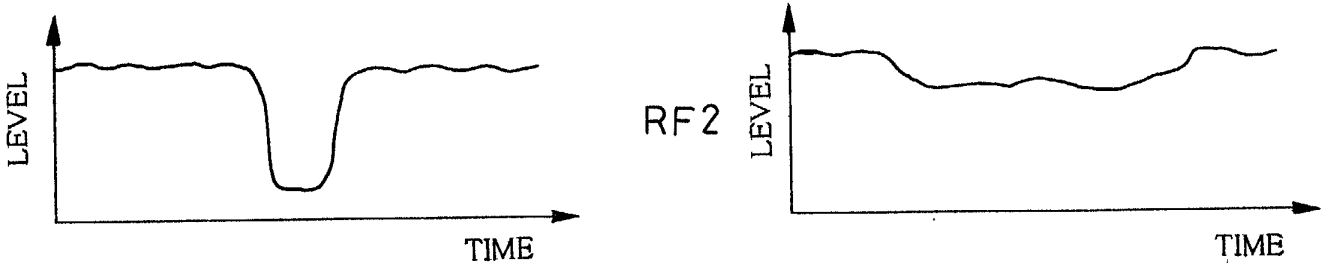


FIG. 7B

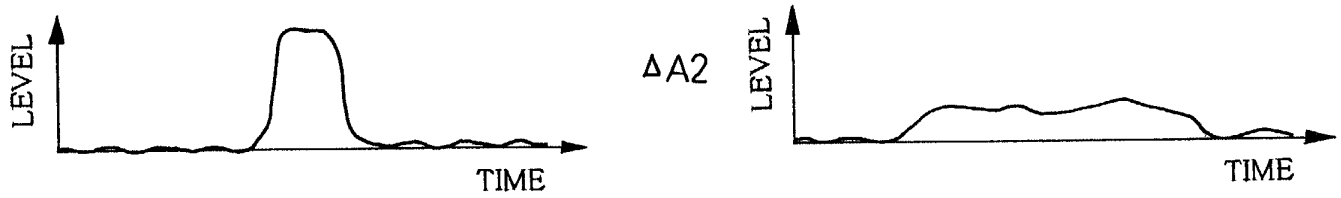


FIG. 7C

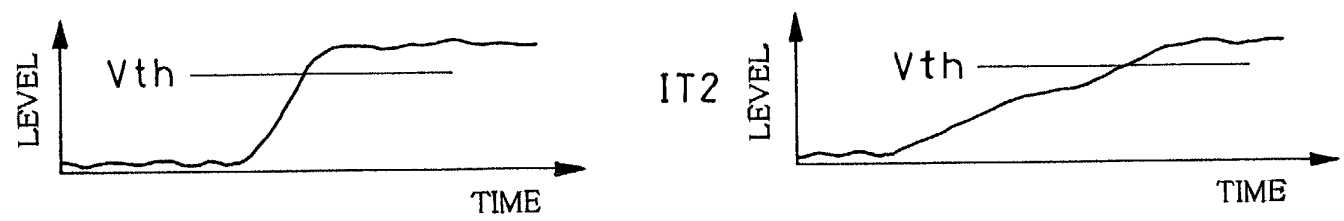


FIG.7D

FIG. 8A

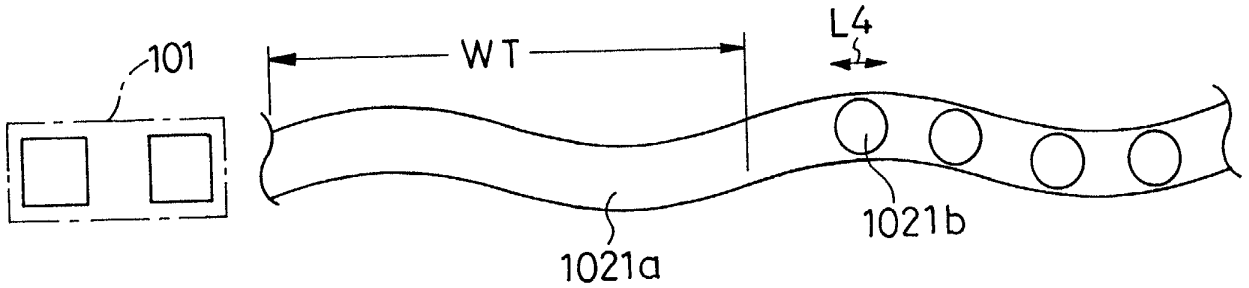


FIG. 8B